Jirong Yang yjrcs@umich.edu | 734-882-8266 | Website

Education

University of Michigan, Ann Arbor Ann Arbor, MI

B.S. in Computer Science **(Honors Track)** and B.S. in Statistics, GPA 3.85/4 2023/08 - 2025/12

Coursework: Computer Architecture*(1st on leaderboard)*, Microarchitecture, Parallel Computer Architecture, Advanced Operating System, Compiler, Parallel Computing, Advanced Machine Learning, Computer Vision, DL for Robotics

Research Interests: My research interests lie at the intersection of architecture and systems, focusing on hardware–software co-design to address application–hardware mismatch and build more coupled domain-specific architectures.

Selected Publication *(* Equal contribution; authors listed alphabetically.)*

H. Jin*, **J. Yang***, B. Lyu, R. Gao, N. Bleier. æSIP: µArch-aware ASIP-ISA Co-Design via Program Synthesis, Equality Saturation, and External Don't Cares. **International Symposium on Computer Architecture (ISCA), 2026.**

H. Jin, **J. Yang**, A. Moreno, R. Gao, B. Lyu, N. Bleier. Scalable Hardware Pruning through Semiformal Verification and Microarchitecture Awareness. **In preparation for ICCAD (manuscript PDF).**

H. Jin, **J. Yang**, Y. Liu, B. Lyu, K. Zhang, N. Bleier. Mozart: A Chiplet Ecosystem-Accelerator Codesign Framework for Composable Bespoke Application Specific Integrated Circuits. **In preparation for MICRO (preprint available).**

T. Liu, **J. Yang**, Y. Yin, M. Li, L. Wang, Z. Zhu. Aligning LLM with human learning and adjustment behavior: a dual agent approach. **Major revision, Transportation Research Part C (preprint available).**

T. Liu, **J. Yang**, Y. Yin. Toward LLM-agent-based modeling of transportation systems: A conceptual framework. **Artificial Intelligence for Transportation, 2025**.

Research Experience

ISA-ASIP Co-Design Research | **Advisor: Prof. Nathan Bleier & Prof. Krisztian Flautner** *2025/08 – 2026/02*

- Built an e-graph–based rewriting system for RV32IM, using block-wise saturation & ILP extraction to tailor ISA subsets.
- Developed a µarch-aware, SVA-based semiformal trimming flow with ~$10^3\times$ speedups and up to 49.6% area reduction.
- Built an ISA–ASIP codesign flow yielding −29.7% area, −8.3% power, +31.6% freq, and −15.6% latency across PPA variants.
- Designed an ecosystem strategy to amortize NRE; 4 ASIPs cut area by 14.17% with +0.23% latency across 20+ programs.
- Validated functional correctness via full Spike compatibility and obtained PnR-verified area/power gains on SKY130.

Chiplet Ecosystem-Accelerator Co-Design Research | **Advisor: Prof. Nathan Bleier** *2025/01 – 2025/08*

- Analyzed operator-level compute–memory mismatch, exposing non-uniform batching and latency–goodput tradeoffs.
- Employed simulated annealing to co-design chiplet pools across dataflows, PE arrays, buffers, and tensor-parallelism.
- Applied genetic search for tensor fusion and memory selection, pruning the space via roofline-guided bandwidth limits.
- Balanced pipeline stages via a DVFS-aware convex-hull method for chiplet integration, with PnR-checked feasibility.
- Identified an 8-chiplet sweet spot via hierarchical DSE, yielding 43.5% energy and 67.7% EDP savings at 91–95% perf.

Real-world Agent Simulation Research | **Advisor: Prof. Yafeng Yin** *2024/05 – 2024/12*

- Built an LLM-agent framework to simulate large-scale travel demand and travel decision-making in urban networks.
- Developed a TextGrad-style framework for personalized LLM agents, aligning agent behaviors with human trajectories.

Work Experience

Software Engineering Intern | **Leju Robotics** *2022/01 – 2022/08*

- Ported a new OS onto a robotics platform, integrated device drivers into kernel, debugged OS–hardware interface issues.
- Developed object-detection module using OpenCV and implemented PID motor control for real-time robot motion.

Projects

N-way Superscalar Out-of-Order R10K Processor | **Advisor: Prof. Krisztian Flautner** 2024/09 - 2024/12

- Developed a high-performance RISC-V CPU in SystemVerilog ***(~20K LOC)***, based on the MIPS R10K architecture.
- Implemented TAGE predictor with early resolution, achieving up to 95% accuracy on standard leaderboard benchmarks.
- Built a speculative LSQ with forwarding and MSHR-based non-blocking I/D-caches, plus prefetching and a victim cache.
- Achieved a 7.8ns critical path (~130 MHz in 25 nm) and ~1.7 CPI across C/assembly benchmarks after synthesis and STA.
- Built a **cycle-level simulator** with automated profiling to identify pipeline and memory hotspots for µarch tuning.

WriteBoost Read-Copy Update (RCU) Library 2024/10 - 2024/12

- Designed an enhanced RCU library with integrated update-side synchronization, simplifying programming model.
- Implemented batch update and object pooling optimizations, enabling amortized copy costs and efficient reclamation.

Award

- S&S Scholarship ($10000) & Summer Undergraduate Research in Engineering (SURE) program ($6000)
- University of Texas at Austin Computer Science Department Distinguished Graduate Fellowship ($40000/year)